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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,855	10/11/2001	Ren-Guey Hsieh	67,200-447	9473
7590	12/15/2004		EXAMINER	
			MOHAMEDULLA, SALEHA R	
			ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/975,855	HSIEH, REN-GUEY
	Examiner	Art Unit
	Saleha R. Mohamedulla	1756

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12 May 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 7,8,16 and 17 is/are allowed.
- 6) Claim(s) 1-6 and 9-15 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-17 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 6, 9-13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US# 5,667,923 to Kanata in view of US# 6,180,289 to Hirayanagi.

3. Kanata teaches that a resist film is formed on a silicon substrate and a charged particle beam exposure is performed thereon (col. 1, lines 19-21). Kanata teaches the exposure pattern will have a parasitic pattern formed due to scattering and that this scattering causes proximity effect (col. 1, lines 27-40). Kanata teaches using electron beam as the charged particle beam (col. 1, lines 40-45). Kanata also teaches substrates used in semiconductor processing (col. 4, lines 4-5). The substrates are coated with various thin-layers such as silicon dioxide and silicon nitride, which are dielectric materials, and aluminum, titanium and tungsten, which are metal materials. Kanata also teaches exposing a resist layer on a substrate formed of various thin layers (col. 4, lines 5-10). Figs. 8A – 10B show selective exposure on a resist film 54 covering a lower level tungsten 52 and an upper level layer 53 (col. 4, lines 25-30). Charged particle beam is irradiated on the resist film according to data of upper level patterns to expose the resist film (col. 4, lines 30-32). Fig. 9B shows the latent image formed in the resist 54. The latent pattern is

contiguous as it is formed in one resist layer. Then, the resist film is developed to form the resist pattern and the upper level layer is etched using the developed resist film as a mask (col. 4, lines 32-35). Figs. 10A and 10B show the resultant structure. The exposed portions of the resist remain on the substrate after development and the pattern of the exposed portions is transferred to the underlying layers shown in Figs. 9B and 10B. Thus, the resist is a negative resist.

Therefore, Kanata teaches providing a substrate, forming over the substrate a blanket target or blanket masking layer, that is, the lower level and/or upper level layer, forming a blanket negative resist layer over the target or masking layer, exposing, while employing a charged particle beam method susceptible to a proximity effect, the resist layer to form a contiguous latent pattern, developing the resist layer to form a patterned resist layer, employing the patterned resist layer as a mask for forming from the blanket target or masking layer a patterned target or masking layer. The substrate can be used in integrated circuit microelectronic fabrications, as the substrate is used in semiconductor processing. The upper and lower level layers can be microelectronic dielectric, such as silicon dioxide or silicon nitride, or microelectronic conductor, such as tungsten, titanium or aluminum, materials. Figures 2 and 3 show that the Kanata relates a direct write method.

Kanata does not teach that the charged beam method employs when forming the latent pattern a series of adjacent fractured pattern elements, where an adjacent pair of pattern elements is separated by a gap.

Hirayanagi teaches a projection microlithography mask for charged particle beam lithography (col. 1, lines 10-20). The mask comprises a pattern defined on a plurality of thin mask reticles. The plurality of mask reticles is secured to a single mask reticle retention member

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(col. 3, lines 1-5). The mask reticle patterns are divided into multiple mask subfields. Each mask subfield comprises a respective portion of the overall pattern to be transferred from the mask to the substrate (col. 3, lines 5-7). Therefore, Hirayanagi teaches that the method employs when exposing a resist layer a series of adjacent fractured pattern elements separated by a gap, that is, the gap formed by the retention member (Fig. 1c; col. 2, lines 5-10). Hirayanagi also teaches alignment marks on the mask reticles and on the retention member (col. 3, lines 7-10). The alignment marks facilitate alignment of the mask and correction of pattern-image errors resulting from mechanically or thermally induced distortion of the mask reticles (col. 3, lines 9-12). Therefore, Hirayanagi teaches that by providing the fractured pattern elements and mask, the sensitive substrate, or resist layer, is formed with enhanced pattern fidelity and critical dimension control, because correct alignment and correction of pattern errors produce enhanced pattern fidelity and critical dimension control.

The references are analogous art as they are drawn to charged particle beam methods. It would have been obvious to one of ordinary skill in the art to use the mask of Hirayanagi in the method of Kanata, as the mask of Hirayanagi can be employed without direct writing which allows for relatively high wafer throughput and decreased costs (Hirayanagi; col. 2, lines 45-50). One of ordinary skill in the art would have a reasonable expectation of success in using the mask of Hirayanagi as Kanata teaches that the charged particle beam method is performed with a mask (Kanata; col. 3, lines 20-22).

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4. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US# 5,667,923 to Kanata in view of US# 6,180,289 to Hirayanagi, as applied to claims 1 and 11 above, in further view of US# 5,629,772 to Ausschnitt.

5. Kanata in view of Hirayanagi teaches the limitations discussed above in paragraph 10. Kanata in view of Hirayanagi teaches a negative resist, but does not teach a positive resist.

Ausschnitt teaches a lithographic process using a mask where a latent image is formed in a photoresist layer (col. 1, lines 15-20). Ausschnitt teaches that the latent image marks the volume of the photoresist material that either is removed during the development process in the case of a positive resist or remains after development in the case of a negative resist (col. 1, lines 25-30).

The references are analogous art as they are drawn to lithographic exposure processes of photosensitive substrates. It would have been obvious to one of ordinary skill in the art to use a positive resist instead of a negative resist as Ausschnitt teaches that it is common in the art to use both negative and positive resists in lithographic exposure processes.

Allowable Subject Matter

6. Claims 7, 8, 16 and 17 are allowed.

Response to Arguments

7. Applicant argues that Hirayanagi does not teach a gap that separates a pair of fractured pattern elements within a series of adjacent fractured pattern elements. Applicant argues that the retention member that the mask reticles are mounted to does not form a gap because the retention

member is in a plane beneath the pair of mask reticles. However, the mask reticles are mask subfields, where each subfield comprises a respective portion of the overall pattern to be transferred from the mask to the substrate (col. 3, lines 5-7). Therefore, each subfield, or mask reticle, is a fractured pattern element. The subfields are separated by a gap (Fig. 1c; col. 2, lines 5-10). There is a space between the subfields therefore a gap exists between the subfields. In addition, the present claims do not recite limitations drawn to the gap being in the same plane as the pattern elements. However, in Hirayanagi the gap occurs in the same plane as the subfields because the space or gap is between the subfields. The drawings, such as Figure 1c, show this feature. Therefore, Applicant's arguments are not persuasive.

Applicant argues that applicant's fractured pattern elements are present within applicant's contiguous latent pattern in the blanket resist layer, as recited in claims 1 and 11. However, this is NOT claimed. The claims recite that the charged particle beam method employs a series of adjacent fractured pattern elements when forming the contiguous latent pattern. The claim does not recite that fractured pattern elements are formed or even present in the contiguous latent pattern. Hirayanagi teaches a mask having fractured pattern elements separated by a gap. Therefore, Hirayanagi teaches a method employing a series of adjacent fractured pattern elements, that is, a method employing a mask with the fractured pattern elements. The presence of these elements in the latent resist image is not a claimed feature of the invention.

Applicant argues that direct writing is required by Kanata and that because of Kanata's teaching, that there is no motivation to combine Kanata and Hirayanagi. However, simply because Hirayanagi discloses exposures in general does not mean that Hirayanagi teaches against direct writing. In addition, nowhere in Kanata is it disclosed that direct writing is required as the

exposure method. Kanata teaches semiconductor wafer exposure using a mask, where the mask pattern is imprinted on the underlying wafer. Hirayanagi also teaches semiconductor wafer exposure using a mask, where the mask pattern is imprinted on the underlying wafer. Therefore, Applicant's arguments are not persuasive.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Saleha Mohamedulla whose telephone number is (571) 272-1387. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Saleha R. Mohamedulla
Patent Examiner
Technology Center 1700
December 12, 2004